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Design for Testability in Timely Testing of Vlsi Circuits

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Abstract
Even though a circuit is designed error-free, manufactured circuits may not function correctly. Since the manufacturing process is not perfect, some defects such as short-circuits, open-circuits, open interconnections, pin shorts, etc., may be introduced. Points out that the cost of detecting a faulty component increases ten times at each step between prepackage component test and system warranty repair. It is important to identify a faulty component as early in the manufacturing process as possible. Therefore, testing has become a very important aspect of any VLSI manufacturing system.Two main issues related to test and security domain are scan-based attacks and misuse of JTAG interface. Design for testability presents effective and timely testing of VLSI circuits. The project is to test the circuits after design and then reduce the area, power, delay and security of misuse. BIST architecture is used to test the circuits effectively compared to scan based testing. In built-in self-test (BIST), on-chip circuitry is added to generate test vectors or analyze output responses or both. BIST is usually performed using pseudorandom pattern generators (PRPGs). Among the advantages of pseudorandom BIST are: (1) the low cost compared to testing from automatic test equipment (ATE). (2) The speed of the test, which is much faster than when it is applied from ATE. (3) The applicability of the test while the circuit is in the field, and (4) the potential for high quality of test.
Keyword: Testing, scan-based attacks, misuse of JTAG interface, BIST.

I. INTRODUCTION

Generally more than one million tests needed to obtain a good fault coverage so testing is very essential to find faulty and good circuits that produces a quality of product. Design for testability (DFT) improves the testability, diagnostics, test time and reduces number of required test pins. Harmful users can use the scan chain to observe confidential data stored in devices by using standard test interface such as JTAG and IEEE 1500.These test interfaces were initially developed for testing printed circuit board or system on chip internal modules but nowadays it is widely used for debugging purposes.

VLSI circuits are tested by applying test patterns to the circuit under test (CUT) and comparing the response of the circuit to the good circuit response, which is obtained by simulation. Design for testability (DFT) techniques are used to improve the controllability (the ability to set the node at a certain value) and the observability (the ability to propagate the value of a node to an observable output) of internal nodes in digital circuits. Among the widely used DFT techniques are scan-path techniques. In scan-path techniques, the circuit is designed to have two modes of operation, namely, a normal functional mode and a test mode. In the test mode, the bistables (the memory elements in the circuit) are interconnected into a shift register. In test mode, it is possible to shift an arbitrary test pattern in the bistables. By going back to the functional mode for one clock pulse, the response of the circuit to the test pattern is latched into the bistables. The circuit can then be placed back in test mode to concurrently shift the response out of the chain and shift a new pattern into the chain. The addition of on-chip circuitry to provide test vectors or to analyze output responses is called built-in self-test (BIST) The pattern generation in BIST is usually done using linear feedback shift registers (LFSRs) or cellular automata (CA).

II. ROLE OF TESTING IN VLSI DESIGN

Even though a circuit is designed error-free, manufactured circuits may not function correctly. Since the manufacturing process is not perfect, some defects such as short circuits, open-circuits, open interconnections, pin shorts, etc., may be introduced. Points out that the cost of detecting a faulty component increases ten times at each step between prepackage component test and system warranty repair. It is important to identify a faulty component as early in the manufacturing process as possible. Therefore, testing has become a very important aspect of any VLSI manufacturing system.

The testing of digital logic involves the application of the appropriate stimuli to a Device Under-Test (DUT) and the comparison of the resulting response to the expected one. Manufacturing defects tend to alter the circuit behavior and, therefore, when the response of a DUT does not match the expected response, it is

considered faulty. For digital circuits, the stimuli are sequences of logic levels 0 and 1, called test patterns or vector that are applied to the inputs of the circuit. Test pattern generation is a complex process with three main aspects: the cost of test generation, the cost of test application and the quality of test.

III. SCAN-BASED ATTACKS

The insertion of scan chains consists of replacing the flip- flops (FFs) of the design by scan flip-flops (SFFs) and connecting these SFFs into a shift-register, called scan chain. The scan chain is bound to a input pin (scan-in) and to an output pin (scan-out). An extra pin called scan-enable should be added to control the scan chain's data shifting. If the scan-enable is set to 0, the SFFs are connected to the circuit to behave as functionally expected (functional mode). When the scan-enable is set to 1, the SFFs are connected to the scan chain, and the bitstream at the scan-in is shifted in while the data stored in the SFFs is shifted out through the scan-out pin. By controlling the scan-in and scan-enable inputs and observing the scan-out pin, and attacker can observe confi- dential data or corrupt internal states. Fig. 1 illustrates the duality between test and security. While the test engineer uses the scan chains to shift-in input patterns and shift-out response vectors, the attacker may shift-out confidential data (observability attacks) and shift-in corrupted data (controllability attacks).

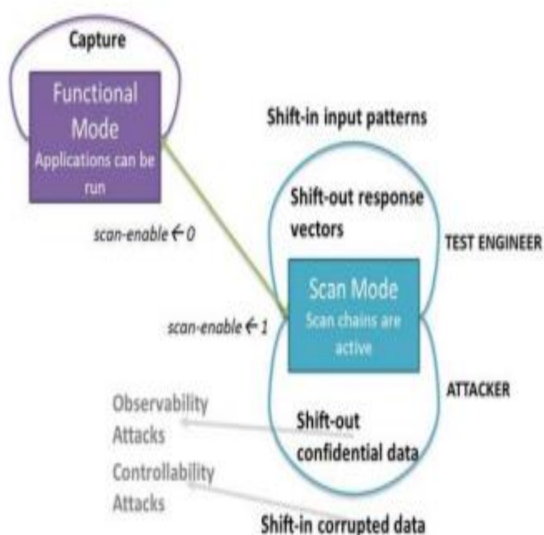

Figure 1 scan based attacks

IV. BIST ARCHITECTURE

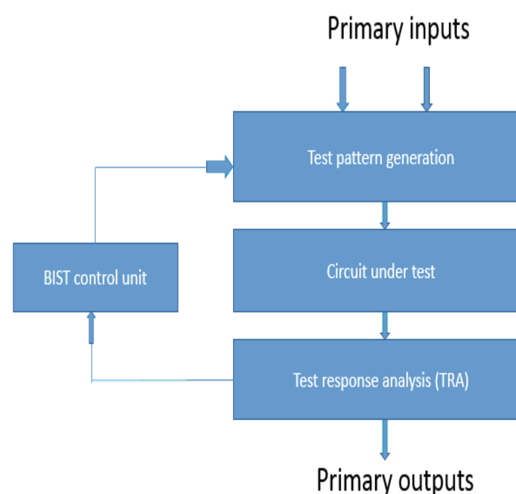

Figure 2 Block diagram of BIST architecture

Test pattern generation generates test patterns with the help of 2:1 MUX and LFSR. It accepts two inputs and produces one output to circuit under test. Circuit under test produces output to test response analysis before that any fault is detected it is just fed back into the BIST control unit and act as a feedback circuit until test end signal is applied. Test response analysis produces good/fault free output.

Advantages

- Reduces testing time.
- Test application time and total energy dissipation during test are improved.
- It reduces delay & power.

V. INTERNAL DIAGRAM OF BIST ARCHITECTURE

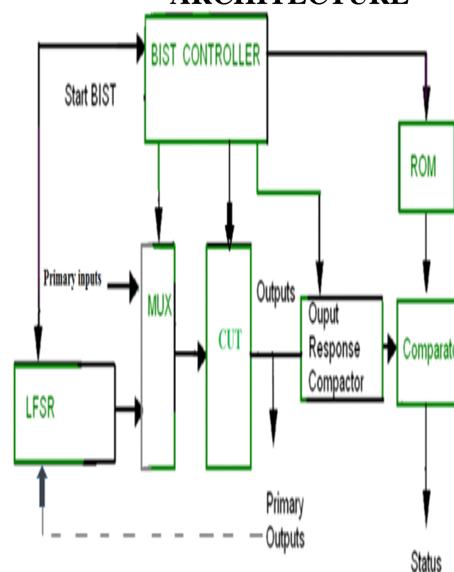

Figure 3 internal diagram

A.BIST CONTROLLER

Whenever an IC is powered up(signal start BIST is made active) the test controller starts the procedure.once the test is over,the status line is made high if fault is found. Following that, the controller connects the primary inputs to the CUT via the multiplexer, thus making it ready for operation.

B.LFSR

Linear feedback shift register act as a feedback circuit. output of CUT is fed back into the LFSR if any faulty or non responsible output present in the CUT output.LFSR reduces the peak power by connecting multiplexer on the LFSR register.LFSR reduces the switching activity in the inputs of the Circuit Under Test.

C.TEST PATTERN GENERATION

Test patterns are generated in the output of multiplexer. The test patterns required to sensitize the faults and then propagate the effect to the outputs of the CUT.

D.CIRCUIT UNDER TEST

Circuit under test produces the primary output which is faulty or any non responsible output.Then the output is fed back into the LFSR in which it act as a feedback circuit, until the test end signal is applied.Remaining outputs are fed into output response compactor.

E.OUTPUT RESPONSE COMPACTOR

Output response compactor performs lossy compression of the outputs of the CUT.Then it produces a fault free signature which describes the good circuit response.During BIST, large amount of data in CUT responses are applied to Response compactor. For example, if we consider a circuit of 200 outputs and if we want to generate 5 million random patterns, then the CUT response to Response compactor will be 1 billion bits. This is not manageable in practice. So it is necessary to compact this enormous amount of circuit responses to a manageable size that can be stored on the chip. The response analyzer compresses a very long test response into a single word. Such a word is called a signature. The signature is then compared with the pre-stored reference signature from ROM with compacted response. If the signature matches the reference copy, the CUT is regarded fault-free. Otherwise, it is faulty.

F.READ ONLY MEMORY

It has reference signature that needs to be compared with the compacted CUT response.

G.COMPARATOR

Hardware to compare compacted CUT response and reference signature (from ROM) and produces the status of the circuit which is good & fault free circuit.

VI. CONCLUSION

Name	Power (W)	Used	Total Available	Utilization (%)
Clocks	0.099	3	--	--
Logic	0.006	232	4896	4.7
Signals	0.156	266	--	--
IOs	3.848	18	172	10.5
Total Quiescent Power	0.117			
Total Dynamic Power	4.204			
Total Power	4.321			

PARAMETER	EXISTING	PROPOSED
Area	90%	75%
Power	4.501 mW	4.321 mW
Delay	16.649ns	16.149ns

In this paper, we have minimized the area,power,delay compared with existing system and simulationresults to find faulty or good circuit by using modelsim –Altera 6.4a software. Advantage of this project is area, power, delay parameters are minimized, testing time is reduced test application time and total energy dissipation during test are improved.

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